

# DATA SHEET

## **74AHC32; 74AHCT32** Quad 2-input OR gate

Product specification  
Supersedes data of 1999 Sep 27

2004 May 19

## Quad 2-input OR gate

## 74AHC32; 74AHCT32

## FEATURES

- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101 exceeds 1000 V.
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accepts voltages higher than  $V_{CC}$
- For 74AHC32 only: operates with CMOS input levels
- For 74AHCT32 only: operates with TTL input levels
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ .

## DESCRIPTION

The 74AHC32; 74AHCT32 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74AHC32; 74AHCT32 provides the 2-input OR function.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f \leq 3.0\text{ ns}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			74AHC32	74AHCT32	
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	2.8	3.1	ns
$C_I$	input capacitance	$V_I = V_{CC}$ or GND	3.0	3.0	pF
$C_O$	output capacitance		4.0	4.0	pF
$C_{PD}$	power dissipation capacitance	$C_L = 50\text{ pF}$ ; $f = 1\text{ MHz}$ ; notes 1 and 2	10	12	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND}$  to  $V_{CC}$ .

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## FUNCTION TABLE

Table 1 See note 1.

INPUT		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

## Note

1. H = HIGH voltage level  
L = LOW voltage level.

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74AHC32D	-40 °C to +125 °C	14	SO14	plastic	SOT108-1
74AHCT32D	-40 °C to +125 °C	14	SO14	plastic	SOT108-1
74AHC32PW	-40 °C to +125 °C	14	TSSOP14	plastic	SOT402-1
74AHCT32PW	-40 °C to +125 °C	14	TSSOP14	plastic	SOT402-1
74AHC32BQ	-40 °C to +125 °C	14	DHVQFN14	plastic	SOT762-1
74AHCT32BQ	-40 °C to +125 °C	14	DHVQFN14	plastic	SOT762-1

## PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1B	data input
3	1Y	data output
4	2A	data input
5	2B	data input
6	2Y	data output
7	GND	ground (0 V)
8	3Y	data output
9	3A	data input
10	3B	data input
11	4Y	data output
12	4A	data input
13	4B	data input
14	V <sub>CC</sub>	supply voltage

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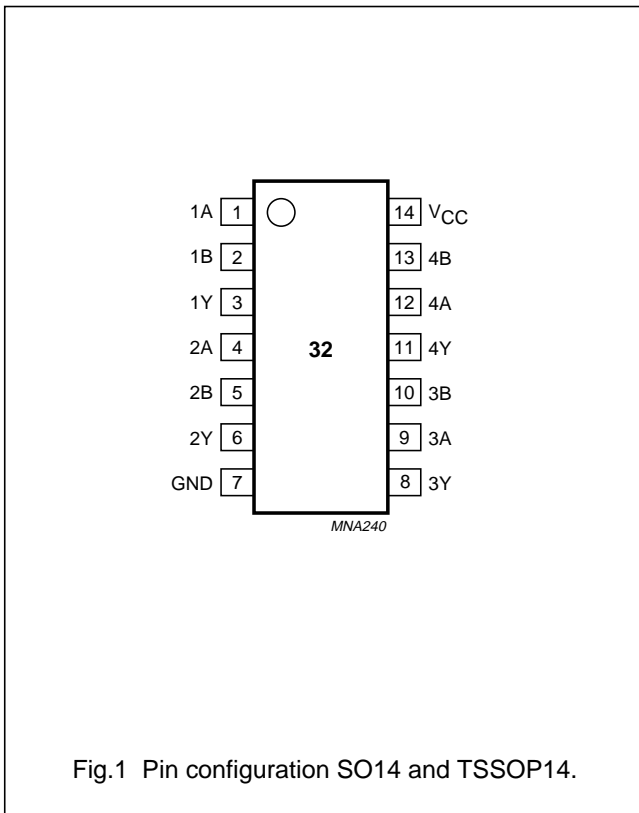


Fig.1 Pin configuration SO14 and TSSOP14.

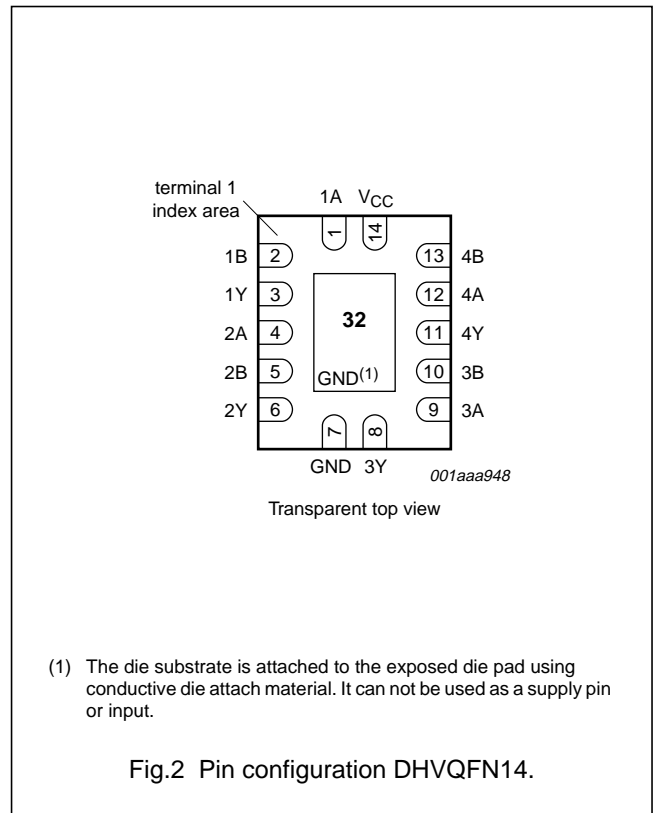


Fig.2 Pin configuration DHVQFN14.

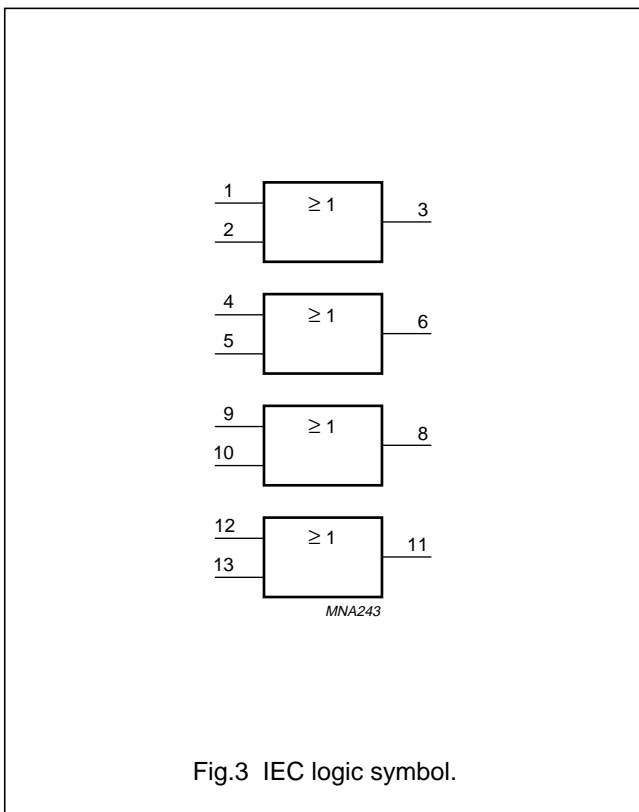


Fig.3 IEC logic symbol.

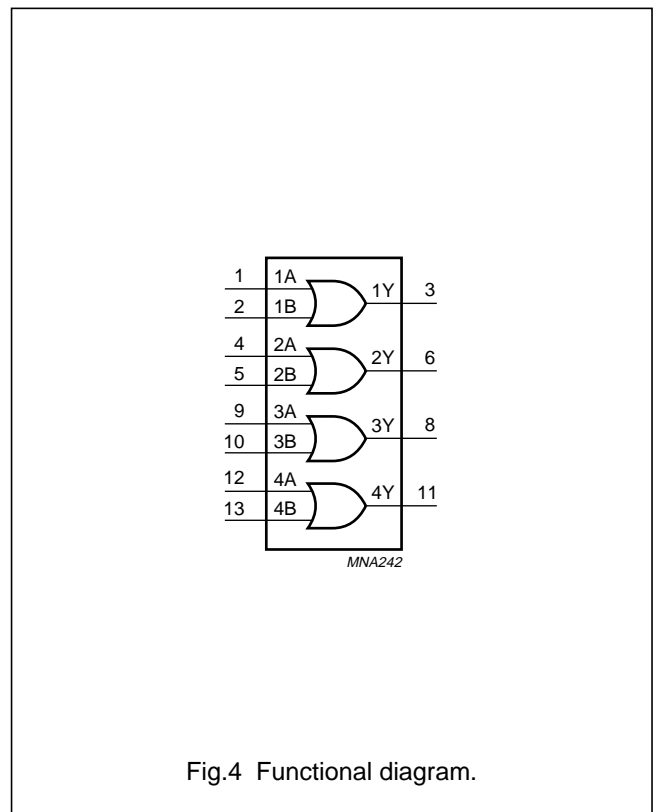


Fig.4 Functional diagram.

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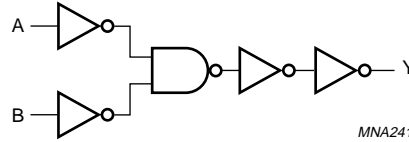


Fig.5 Logic diagram (one gate).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC32			74AHCT32			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V <sub>CC</sub>	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	–	5.5	0	–	5.5	V
V <sub>O</sub>	output voltage		0	–	V <sub>CC</sub>	0	–	V <sub>CC</sub>	V
T <sub>amb</sub>	operating ambient temperature		–40	+25	+125	–40	+25	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times	V <sub>CC</sub> = 3.3 V ± 0.3 V	–	–	100	–	–	–	ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V	–	–	20	–	–	20	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		–0.5	+7.0	V
V <sub>I</sub>	input voltage		–0.5	+7.0	V
I <sub>IK</sub>	input diode current	V <sub>I</sub> < –0.5 V; note 1	–	–20	mA
I <sub>OK</sub>	output diode current	V <sub>O</sub> < –0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V; note 1	–	±20	mA
I <sub>O</sub>	output source or sink current	V <sub>O</sub> > –0.5 V and V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	–	±25	mA
I <sub>CC</sub> , I <sub>GND</sub>	V <sub>CC</sub> or GND current		–	±75	mA
T <sub>stg</sub>	storage temperature		–65	+150	°C
P <sub>tot</sub>	power dissipation	T <sub>amb</sub> = –40 °C to +125 °C; note 2	–	500	mW

Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO14 packages: above 70 °C the value of P<sub>tot</sub> derates linearly with 8 mW/K.  
 For TSSOP14 packages: above 60 °C the value of P<sub>tot</sub> derates linearly with 5.5 mW/K.  
 For DHVQFN14 packages: above 60 °C the value of P<sub>tot</sub> derate linearly with 4.5 mW/K.

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## DC CHARACTERISTICS

## Type 74AHC32

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = 25 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = –50 µA; all outputs	2.0	1.9	2.0	–	V
		I <sub>O</sub> = –50 µA; all outputs	3.0	2.9	3.0	–	V
		I <sub>O</sub> = –50 µA; all outputs	4.5	4.4	4.5	–	V
		I <sub>O</sub> = –4.0 mA	3.0	2.58	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = 50 µA; all outputs	2.0	–	0	0.1	V
		I <sub>O</sub> = 50 µA; all outputs	3.0	–	0	0.1	V
		I <sub>O</sub> = 50 µA; all outputs	4.5	–	0	0.1	V
		I <sub>O</sub> = 4.0 mA	3.0	–	–	0.36	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	0.1	µA
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	–	–	±0.25	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	–	2.0	µA
C <sub>I</sub>	input capacitance		–	–	3	10	pF

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -50 µA; all outputs	2.0	1.9	–	–	V
		I <sub>O</sub> = -50 µA; all outputs	3.0	2.9	–	–	V
		I <sub>O</sub> = -50 µA; all outputs	4.5	4.4	–	–	V
		I <sub>O</sub> = -4.0 mA	3.0	2.48	–	–	V
		I <sub>O</sub> = -8.0 mA	4.5	3.8	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 50 µA; all outputs	2.0	–	–	0.1	V
		I <sub>O</sub> = 50 µA; all outputs	3.0	–	–	0.1	V
		I <sub>O</sub> = 50 µA; all outputs	4.5	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	3.0	–	–	0.44	V
		I <sub>O</sub> = 8.0 mA	4.5	–	–	0.44	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	1.0	µA
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	–	–	±2.5	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	–	20	µA
C <sub>I</sub>	input capacitance		–	–	–	10	pF

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -50 µA; all outputs	2.0	1.9	–	–	V
		I <sub>O</sub> = -50 µA; all outputs	3.0	2.9	–	–	V
		I <sub>O</sub> = -50 µA; all outputs	4.5	4.4	–	–	V
		I <sub>O</sub> = -4.0 mA	3.0	2.40	–	–	V
		I <sub>O</sub> = -8.0 mA	4.5	3.70	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 50 µA; all outputs	2.0	–	–	0.1	V
		I <sub>O</sub> = 50 µA; all outputs	3.0	–	–	0.1	V
		I <sub>O</sub> = 50 µA; all outputs	4.5	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	3.0	–	–	0.55	V
		I <sub>O</sub> = 8.0 mA	4.5	–	–	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	2.0	µA
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	–	–	±10.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	–	40	µA
C <sub>I</sub>	input capacitance		–	–	–	10	pF



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## Type 74AHCT32

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = 25 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –50 µA; all outputs I <sub>O</sub> = –8.0 mA	4.5	4.4	4.5	–	V
			4.5	3.94	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 50 µA; all outputs I <sub>O</sub> = 8.0 mA	4.5	–	0	0.1	V
			4.5	–	–	0.36	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	5.5	–	–	0.1	µA
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND per input pin; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	–	±0.25	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	–	2.0	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> – 2.1 V other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	4.5 to 5.5	–	–	1.35	mA
C <sub>I</sub>	input capacitance		–	–	3	10	pF
<b>T<sub>amb</sub> = –40 °C to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –50 µA; all outputs I <sub>O</sub> = –8.0 mA	4.5	4.4	–	–	V
			4.5	3.8	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 50 µA; all outputs I <sub>O</sub> = 8.0 mA	4.5	–	–	0.1	V
			4.5	–	–	0.44	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	5.5	–	–	1.0	µA
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND per input pin; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	–	±2.5	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	–	20	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> – 2.1 V other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	4.5 to 5.5	–	–	1.5	mA
C <sub>I</sub>	input capacitance		–	–	–	10	pF

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = -50 µA; all outputs I <sub>O</sub> = -8.0 mA	4.5 4.5	4.4 3.70	– –	– –	V V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = 50 µA; all outputs I <sub>O</sub> = 8.0 mA	4.5 4.5	– –	– –	0.1 0.55	V V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	5.5	–	–	2.0	µA
I <sub>OZ</sub>	3-state output OFF current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND per input pin; other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	–	±10.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	–	40	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	4.5 to 5.5	–	–	1.5	mA
C <sub>I</sub>	input capacitance		–	–	–	10	pF

## Quad 2-input OR gate

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## AC CHARACTERISTICS

## Type 74AHC32

GND = 0 V;  $t_r = t_f \leq 3.0$  ns; see Fig.7.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	$C_L$				
<b><math>T_{amb} = 25\text{ }^\circ\text{C}</math></b>							
<b><math>V_{CC} = 3.0\text{ V to }3.6\text{ V}</math>; note 1</b>							
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	see Fig.6	15 pF	–	3.9	7.9	ns
			50 pF	–	5.6	11.4	ns
<b><math>V_{CC} = 4.5\text{ V to }5.5\text{ V}</math>; note 2</b>							
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	see Fig.6	15 pF	–	2.8	5.5	ns
			50 pF	–	4.1	7.5	ns
<b><math>T_{amb} = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}</math></b>							
<b><math>V_{CC} = 3.0\text{ V to }3.6\text{ V}</math></b>							
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	see Fig.6	15 pF	1.0	–	9.5	ns
			50 pF	1.0	–	13	ns
<b><math>V_{CC} = 4.5\text{ V to }5.5\text{ V}</math></b>							
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	see Fig.6	15 pF	1.0	–	6.5	ns
			50 pF	1.0	–	8.5	ns
<b><math>T_{amb} = -40\text{ }^\circ\text{C to }+125\text{ }^\circ\text{C}</math></b>							
<b><math>V_{CC} = 3.0\text{ V to }3.6\text{ V}</math></b>							
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	see Fig.6	15 pF	1.0	–	10.0	ns
			50 pF	1.0	–	14.5	ns
<b><math>V_{CC} = 4.5\text{ V to }5.5\text{ V}</math></b>							
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	see Fig.6	15 pF	1.0	–	7.0	ns
			50 pF	1.0	–	9.5	ns

## Notes

1. Typical values are measured at  $V_{CC} = 3.3\text{ V}$ .
2. Typical values are measured at  $V_{CC} = 5.0\text{ V}$ .

## Quad 2-input OR gate

## 74AHC32; 74AHCT32

**Type 74AHCT32**GND = 0 V;  $t_r = t_f \leq 3.0$  ns; see Fig.7.

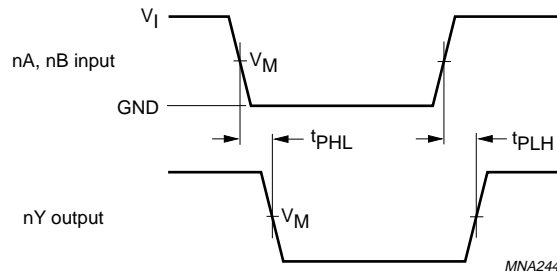
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	$C_L$				
<b><math>T_{amb} = 25\text{ °C}</math></b>							
<b><math>V_{CC} = 4.5\text{ V to }5.5\text{ V}</math>; note 1</b>							
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	see Fig.6	15 pF	–	3.1	6.9	ns
			50 pF	–	4.3	7.9	ns
<b><math>T_{amb} = -40\text{ °C to }+85\text{ °C}</math></b>							
<b><math>V_{CC} = 4.5\text{ V to }5.5\text{ V}</math></b>							
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	see Fig.6	15 pF	1.0	–	8.0	ns
			50 pF	1.0	–	9.0	ns
<b><math>T_{amb} = -40\text{ °C to }+125\text{ °C}</math></b>							
<b><math>V_{CC} = 4.5\text{ V to }5.5\text{ V}</math></b>							
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	see Fig.6	15 pF	1.0	–	9.0	ns
			50 pF	1.0	–	10.0	ns

**Note**1. Typical values are measured at  $V_{CC} = 5.0$  V.

Quad 2-input OR gate

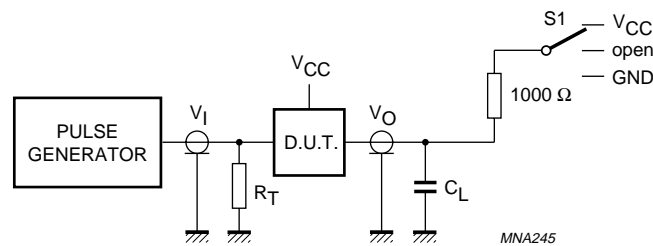
74AHC32; 74AHCT32

AC WAVEFORMS



FAMILY	V <sub>I</sub> INPUT REQUIREMENTS	V <sub>M</sub> INPUT	V <sub>M</sub> OUTPUT
AHC	GND to V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>
AHCT	GND to 3.0 V	1.5 V	0.5 × V <sub>CC</sub>

Fig.6 The input (nA, nB) to output (nY) propagation delays.



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>CC</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

Definitions for test circuit:  
 C<sub>L</sub> = load capacitance including jig and probe capacitance.  
 R<sub>T</sub> = termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.7 Load circuitry for switching times.

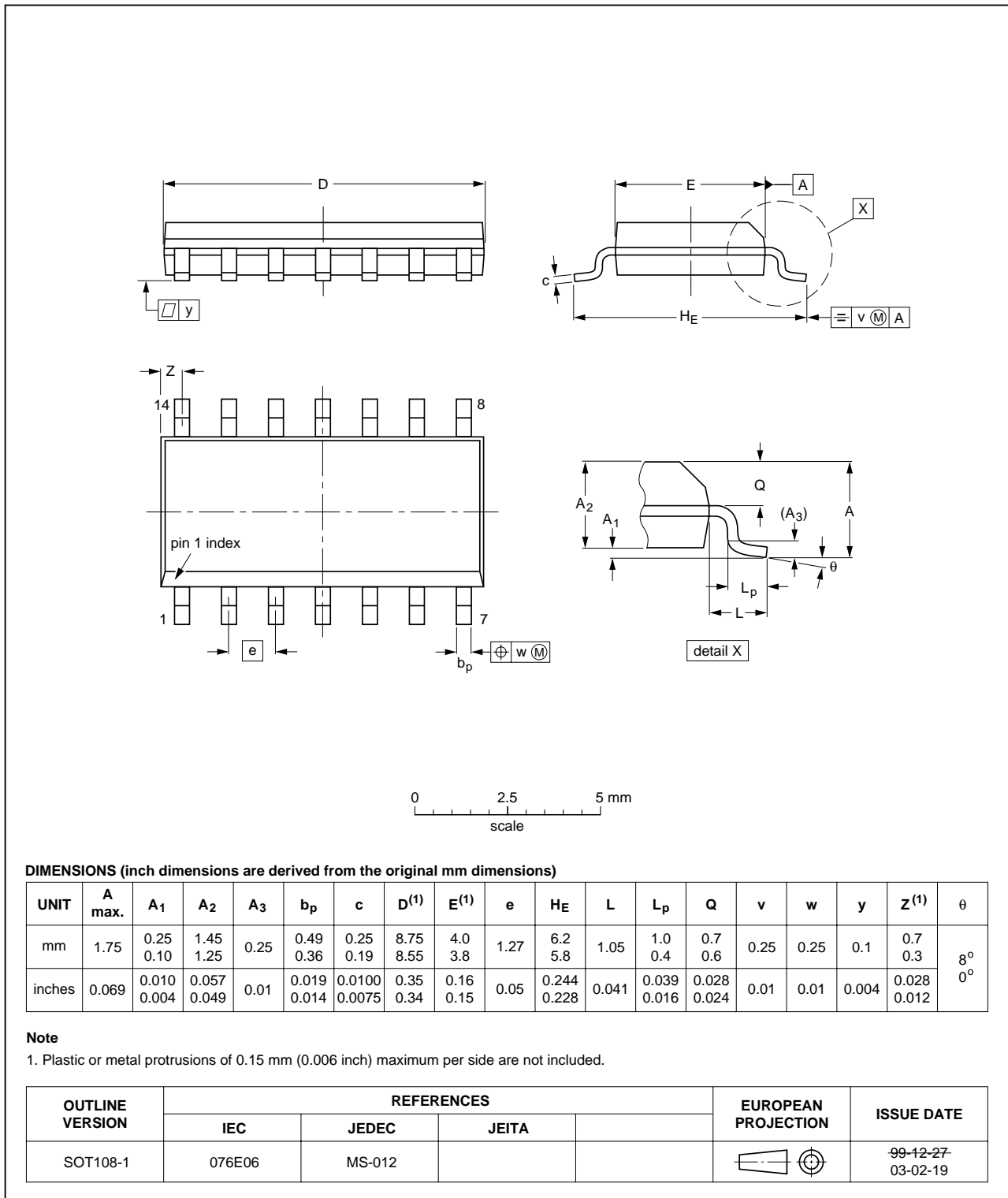
Quad 2-input OR gate

74AHC32; 74AHCT32

PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

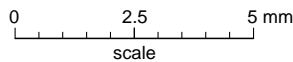
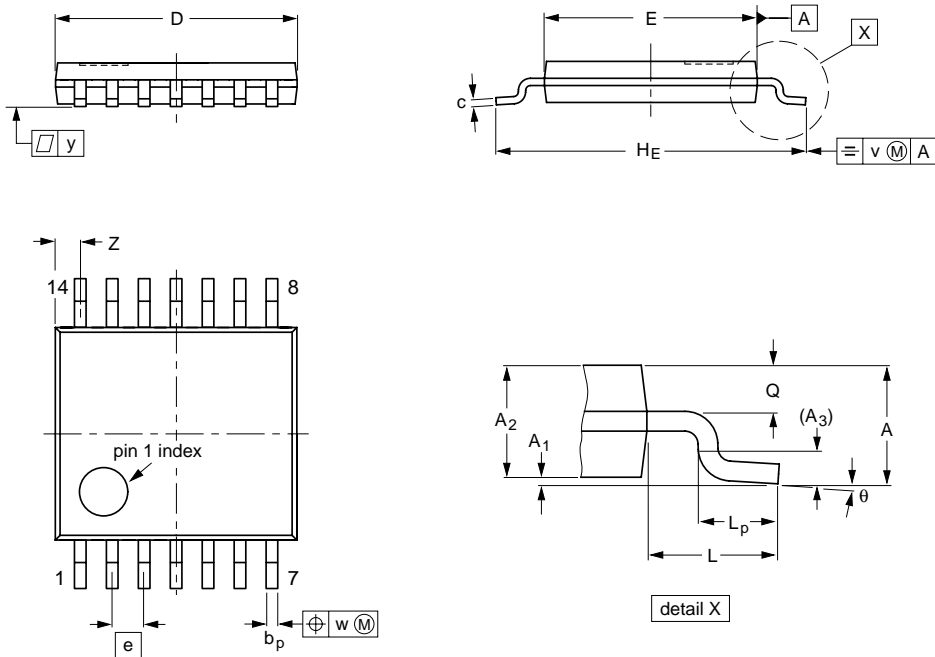


Quad 2-input OR gate

74AHC32; 74AHCT32

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

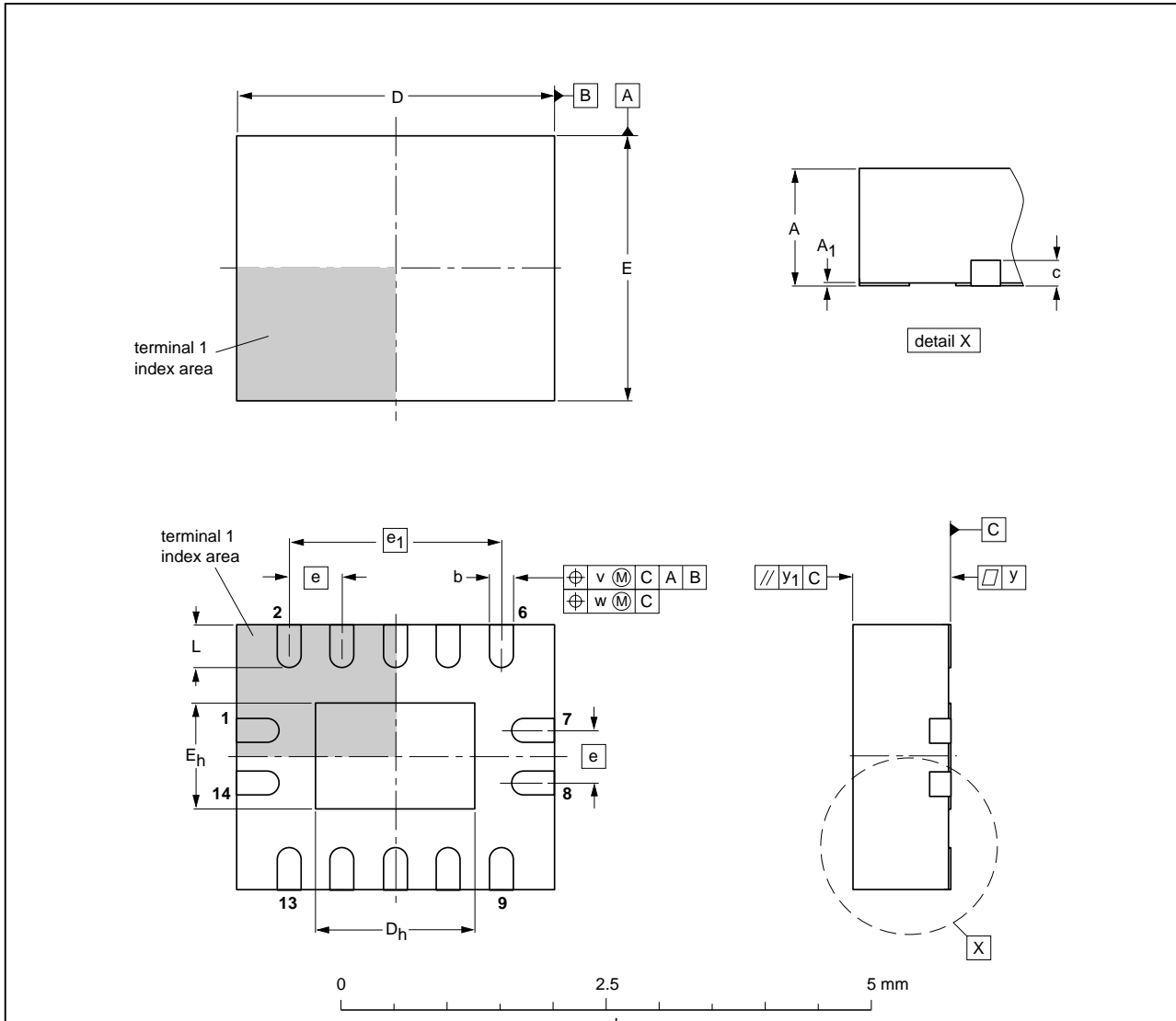
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT402-1		MO-153			99-12-27 03-02-18

Quad 2-input OR gate

74AHC32; 74AHCT32

**DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm**

**SOT762-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sup>(1)</sup> max.	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	L	v	w	y	y <sub>1</sub>
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT762-1	---	MO-241	---		02-10-17 03-01-27



## Quad 2-input OR gate

## 74AHC32; 74AHCT32

## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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